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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/461,643	12/14/1999	KEITH DOW	10559/108001	4089

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/461,643	Applicant(s) DOW, KEITH	
	Examiner Christopher E. Lee	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/14/2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10-14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of the Amendment filed 14th of August, 2002. Claims 1, 4-6, 8, 12-14, and 16-20 have been amended; claims 2, 9 and 15 have been canceled; and claims 21 and 22 have been newly added. Currently, claims 1, 3-8, 10-14, and 16-22 are pending in this application.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Specification

3. The use of the trademark Rambus has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 112

4. Claims 5,6,13,15-17, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "about" in claims 6, 13, 19 is a relative term which renders the claim indefinite.

The term "roughly" in claims 15-17 is a relative term which renders the claim indefinite.

The term "approximately" in claim 5 is a relative term which renders the claim indefinite. Those terms are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

5. Claims 1,3,7,8,10,14,16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] in view of Kumakura et al.[USPN 6,114,751] and AAPA [Applicant Admitted Prior Art; hereinafter AAPA].

Referring to claim 1, Boaz et al. disclose a computer system (Fig. 1) comprising: processor (microprocessor 12); a memory unit (Rambus memory chip 21) configured to store data used by said processor (i.e., as system memory 64); a memory control unit (memory controller 15) configured to manage data flowing into and out of said memory unit (i.e., being coupled with said memory unit); a circuit board (motherboard 10 and RIMM PCB-Rambus In-line Memory Module Printed Circuit Board 17 as combined) having multiple layers (See Fig. 2-3 and col. 2, lines 40, 59) and comprising: a first signal line (i.e., signal lines from said memory control unit 15 to a Rambus memory chip 21 by way of the signal lines on said mother board and said RIMM Circuit Board 17, as combined), formed on a first layer (Fig. 3) of said circuit board and connected (See Fig. 1-3, col. 2, lines 27-65) between a first connection (a connection point of a route 24 and a pin of said Rambus memory chip 21 in Fig. 3) on said memory unit and said memory control unit; and a second signal line (i.e., signal lines from said Rambus memory chip 21 to another Rambus memory chip 21 on said RIMM Circuit Board 17, as combined) also formed on said first layer of said circuit board and connected to said first connection (said connection point of said route 24 and said pin of said Rambus memory chip 21 in Fig. 3) on said memory unit, wherein said first layer defines a non-grounded gap between said first and second signal lines (See Fig. 3 and col. 4, lines 58-60; i.e., wherein in fact that the ground may be located in another layer implies said first layer defining a non-grounded gap between said first and second signal lines since its necessary ground lines are in another layer). Boaz et al. do not disclose a first portion of said second signal line substantially parallel to a first portion of said first signal line. Kumakura et al. disclose a printed circuit board with plural bus channel lines running in parallel with each other (Fig. 25-26), wherein a portion of a signal line substantially parallel (See col. 19, lines 42-47) to a portion of another signal line (See col.19, lines 35+; i.e., wherein in fact that the pitch of the bus channel lines is 0.25mm(10 mils) or 0.375mm(14.75 mils implies a portion of a signal line (i.e., a first bus channel line) substantially parallel to a portion of another signal line (i.e., a second bus channel line)). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said parallel routing technique, as disclosed by Kumakura et al., to said circuit board routing, as disclosed by Boaz et al., for the advantage

of reducing a routing congestion at said memory unit. Boaz et al., as modified by Kumakura et al., do not teach a second portion of said second signal line at an acute angle relative to a second portion of said first signal line. AAPA teaches a portion of a signal line at an acute angle relative to a portion of another signal line (See the angular relationship between the signal line 150,160 and the pin 155 in Fig. 2; Note the definition of the term "acute" in dictionary states -ending in a sharp point: as being or forming an angle measuring less than 90 degrees-, Merriam Webster's Colligiate Dictionary by Merriam-Webster, Inc."). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said acute angle routing technique, as disclosed by AAPA, to said circuit board routing, as disclosed by Boaz et al. in view of Kumakura et al., for the advantage of minimizing an inductive cross-talk noise (See col. 14, line 59 through col. 15, line 9 of Kumakura et al.).

Referring to claim 3, Boaz et al. disclose third and fourth signal lines (i.e., signal routes on the layer in Fig. 4), on a second layer of said circuit board, different than said first layer (See col. 2, lines 6-9 and Fig. 3,4).

Referring to claim 7, Boaz et al. disclose said memory unit (Rambus memory chip 21) is a Rambus device.

Referring to claim 8, the method steps of claim 8 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 8.

Referring to claim 10, the method steps of claim 10 are inherently performed by the apparatus of claim 3, and therefore the rejection of claim 3 applies to claim 10.

Referring to claim 14, the method steps of claim 14 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 14.

Referring to claim 16, the method steps of claim 16 are inherently performed by the apparatus of claim 3, and therefore the rejection of claim 3 applies to claim 16.

Referring to claim 22, Boaz et al. disclose said first connection on said memory unit comprises a pin connection (i.e., a connection point of a route 24 and **a pin of said Rambus memory chip** 21 in Fig. 3).

6. Claims 4,5,11,12,17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] in view of Kumakura et al.[USPN 6,114,751] and AAPA as applied to claim 1 above, and further in view of Perino et al.[USPN 6,160,716].

Referring to claims 4 and 5, Boaz et al., as modified by Kumakura et al.[USPN 6,114,751] and AAPA, disclose all the limitations of claims 4 and 5 except that do not expressly teach that the portion of said second signal line (1) have equal widths, and (2) are separated by a distance equal to said widths. Perino et al. disclose the width of signal trace on a circuit board is determined based on the impedance to be matched (See col.5, lines 48-49). The claim clearly defines that said signal lines are connected on said memory unit. And, the dielectric thicknesses of said circuit board layer for both of said signal lines are same because both of them are on said first layer. In addition, Perino et al. disclose the distance spacing is also affecting the value of line impedance (See col.5, lines 37-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width determination, as disclosed by Perino et al., to said circuit board routing, as disclosed by Boaz et al. in view of Kumakura et al. and AAPA, so that (1) the signal line widths of said first and second signal lines are equal because the determined impedance values should be same, and (2) said portion of said signal lines has set the separating distance equal to said width, for the advantage of (1) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See col. 5 lines 29-32 from Perino et al.), and (2) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See col. 5 lines 29-32 from Perino et al.).

Referring to claim 11, the method steps of claim 11 are inherently performed by the apparatus of claim 4, and therefore the rejection of claim 4 applies to claim 11.

Referring to claim 12, the method steps of claim 12 are inherently performed by the apparatus of claim 5, and therefore the rejection of claim 5 applies to claim 12.

Referring to claim 17, the method steps of claim 17 are inherently performed by the apparatus of claim 4, and therefore the rejection of claim 4 applies to claim 17.

Referring to claim 18, the method steps of claim 18 are inherently performed by the apparatus of claim 5, and therefore the rejection of claim 5 applies to claim 18.

7. Claims 6,13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] in view of Kumakura et al.[USPN 6,114,751] and AAPA as applied to claim 1 above, and further in view of Holman et al.[USPN 6,005,776].

Referring to claim 6, Boaz et al., as modified by Boaz et al. in view of Kumakura et al. and AAPA, disclose all the limitations of claim 6 except that do not teach said signal lines and said separate distance between them are each 5 mils. Holman et al. teach that PCB technology may include conventional "5/5 routing rules" (See col. 3 lines 60-62) which requires 5 mils spacing between each transmission line and neighboring connection leads. Also, Holman et al. discloses an example which shows 5 mil spacing and 5 mil width of transmission line (See Fig. 4, col.4, lines 15-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the 5 mils line width and spacing, as disclosed by Holman et al., to said circuit board routing, as disclosed by Boaz et al. in view of Kumakura et al. and AAPA, so that said widths of said lines and said distance separating said lines are set each 5 mils, for the advantage of providing a sufficient space between neighboring connection in general (See col. 4, lines 15-25).

Referring to claim 13, the method steps of claim 13 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 13.

Referring to claim 19, the method steps of claim 19 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 19.

8. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leddige et al.[USPN 6,111,205] in view of Kumakura et al.[USPN 6,114,751], AAPA and Boaz et al.[USPN 6,061,263].

Leddige et al. disclose a circuit board 100 (Fig. 1) for use in a computer system (See col. 3, lines 24-42; i.e., said circuit board could be used in a computer as a memory unit part) comprising: a memory unit (memory device 110); a memory control unit (memory controller 120); and a data bus (signal traces

130) connecting said memory unit (memory device 110) to said memory control unit (memory controller 120) and comprising: a first signal line (signal traces 130) formed on a selected layer of said circuit board 100 and connected to said memory control unit (memory controller 120) and to a first connection on said memory unit (memory device 110); and a second signal line (signal traces 130) formed on said selected layer of said circuit board and also connected to said first connection on said memory unit (memory device 110). Leddige et al. do not disclose a first portion of said second signal line substantially parallel to a first portion of said first signal line. Kumakura et al. disclose a printed circuit board with plural bus channel lines running in parallel with each other (Fig. 25-26), wherein a portion of a signal line substantially parallel (See col. 19, lines 42-47) to a portion of another signal line (See col.19, lines 35+; i.e., wherein in fact that the pitch of the bus channel lines is 0.25mm(10 mils) or 0.375mm(14.75 mils implies a portion of a signal line (i.e., a first bus channel line) substantially parallel to a portion of another signal line (i.e., a second bus channel line)). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said parallel routing technique, as disclosed by Kumakura et al., to said circuit board routing, as disclosed by Leddige et al., for the advantage of reducing a routing congestion at said memory unit. Leddige et al., as modified by Kumakura et al., do not teach a second portion of said second signal line at an acute angle relative to a second portion of said first signal line. AAPA teaches a portion of a signal line at an acute angle relative to a portion of another signal line (See the angular relationship between the signal line 150,160 and the pin 155 in Fig. 2; Note the definition of the term "acute" in dictionary states -ending in a sharp point: as being or forming an angle measuring less than 90 degrees-, Merriam Webster's Colligiate Dictionary by Merriam-Webster, Inc."). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said acute angle routing technique, as disclosed by AAPA, to said circuit board routing, as disclosed by Leddige et al. in view of Kumakura et al., for the advantage of minimizing an inductive cross-talk noise (See col. 14, line 59 through col. 15, line 9 of Kumakura et al.). Leddige et al., as modified by Kumakura and AAPA, do not teach wherein, said selected layer defines a non-grounded gap between said first and second lines. Boaz et al. teach wherein, said first layer

defines a non-grounded gap between said first and second signal lines (See Fig. 3 and col. 4, lines 58-60; i.e., wherein in fact that the ground may be located in another layer implies said first layer defining a non-grounded gap between said first and second signal lines since its necessary ground lines are in another layer). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied said separated ground layer routing (i.e., non-grounded gap on a signal layer) technique, as disclosed by Boaz et al., to said circuit board routing, as disclosed by Leddige et al. in view of Kumakura et al. and AAPA, for the advantage of offering a signal integrity and routing advantages and lessening a significance of differences in inductance between pins on the top and bottom of said circuit board (See col. 5, lines 7-13 from Boaz et al.).

Referring to claim 21, Boaz et al. disclose said first connection comprises a pin connection (i.e., a connection point of a route 24 and **a pin of said Rambus memory chip** 21 in Fig. 3).

Response to Arguments

9. Applicant's arguments filed 8th of August, 2002 with respect to claims 1, 3-8, 10-14, and 16-22 have been considered but are moot in view of the new ground(s) of rejection.

In response to applicant argument with respect to "neither Boaz nor Leddige, and none of the other art cited teaches or suggests "a circuit board...and second lines", as recited by Applicant's exemplary claim 1. And the other independent claims 8, 14 and 20, having similar limitations to independent claim 1 are not taught by the aforementioned references. Therefore, all the pending claims including the dependent claims are in condition of allowance". The examiner brought AAPA (Applicant Admitted Prior Art) reference in the rejection for the limitations which are not provided by Boaz, Leddige, and all of the other art cited (See *Claim Rejections - 35 USC § 103*).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter S. Wong can be reached on 703-305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3718 for regular communications and 703-746-9248 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2181

cel/ CEL
September 3, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
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